Amendment to the Specification:

Please replace the paragraph beginning on page 5, line 24, and ending on page 6, line 4, with the following paragraph:

--In the operation of processor validation system 200, program 210 is executed on high level simulator 220, which generates state data. Next, checkpoint generator 230 establishes a plurality of checkpoints, checkpoint 1, checkpoint 2, and checkpoint N. Then, state data, state data 1, state data 2, and state data N, at each of the checkpoints, is saved in storage unit 240. Finally, program 210 is run on the plurality of low level simulators 252, 254, 256, in parallel, where each of low level simulators 252, 254, 256, is started at a corresponding checkpoint (checkpoint 1, checkpoint 2, checkpoint N) with corresponding state data (state data 1, state data 2, state data N) associated with the corresponding checkpoint. For example, low level simulator 252, designated as low level simulator 1, is started at its corresponding checkpoint 1 with its corresponding state data 1. In a further embodiment, the plurality of checkpoints, checkpoint 1, checkpoint 2, and checkpoint N, is saved in storage unit 240. In another embodiment program 210 is run on one low level simulator where the low level simulator is started at a checkpoint with state data associated with the checkpoint.--

Please replace the paragraph beginning on page 10, line 23 and ending on page 11, line 9, with the following paragraph:

--Figure 5 is a block diagram of the memory 500 of a low level simulator 252, 254, 256 in an embodiment of the present invention. Memory 500 includes a register memory 510, a cache memory 520, a main memory 530, and a branch prediction memory 540. In a specific embodiment, register memory 510 includes the register contents of the processor. In another embodiment, cache memory 520 includes the cache memory contents of the processor. In a further embodiment, main memory 530 includes the main memory contents of the processor. In a different embodiment, branch prediction memory 540 includes the branch prediction contents of the processor. For example, in a low level simulator, (1) memory locations 1 to 100

may be allocated to register memory 510, (2) memory locations 101 to 200 may be allocated to cache memory 520, (3) memory locations 201 to 1000 may be allocated to main memory 530, and (4) memory locations 1001 to 1100 may be allocated to branch prediction memory 540. In another embodiment, memory 500 includes a program counter memory. In a specific embodiment, the program counter memory includes the program counter contents of the processor. For example, memory locations 1101 to 1200 may be allocated to the program counter memory. In another embodiment, memory 500 includes a value prediction memory. In a specific embodiment, the value prediction memory includes the value prediction contents of the processor. For example, memory locations 1201 to 1300 may be allocated to the value prediction memory.--